# NCS5652, NCV5652

# Dual Power Operational Amplifier

### Description

The NCx5652 is a dual power operational amplifier with a versatile output stage configuration that allows conventional op−amp biasing or user tuning of efficiency, isolation, or current monitoring. Integrated flyback diodes protect the amplifiers during inductive load transients. Operating at supply voltages as low as 3.3 V, the NCx5652 is capable of delivering 500 mA of current while maintaining an excellent output swing. The integrated thermal shutdown circuit protects the NCx5652 from excessive power dissipation. A thermal warning flag is provided for external monitoring of the device, providing a flexible interface to a system's microcontroller. This open−collector thermal flag output doubles as a $\overline{\text{DISABLE}}$ input that can be used to tri−state both amplifier outputs under user control. The 12−pin UDFN 3x3 mm package provides thermal robustness while achieving space savings on high density PCBs.

### Features

- Operating Supply Voltage Range: 3.3 V to 13.2 V
- Output Supply Voltage Range: 3.3 V to 13.2 V
- High Current Drive: 500 mA Operating
- Thermal Flag: Open−collector for Flexible Interface
- Thermal Shutdown/ Disable Function
- Output Short Circuit Tolerable (1 A to Source or Ground)
- No Power Sequencing Required ($V_{CC}$, VC1, VC2)
- UDFN−12 Package Features Wettable Flank for Improved Solderability
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Telecom
- Vcom Driver
- Small DC Brush Motors
- LED String Driver
- Electrochromic Driver

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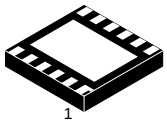
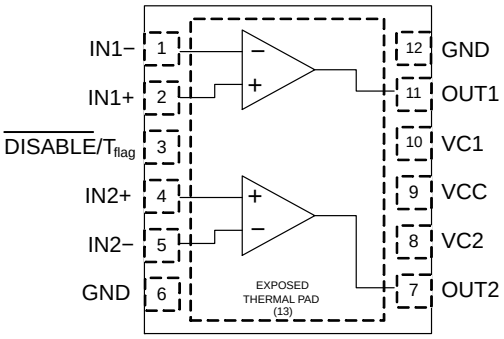



**UDFN12**
**MU SUFFIX**
**CASE 517AM**

### MARKING DIAGRAM


N5652 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)




### ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

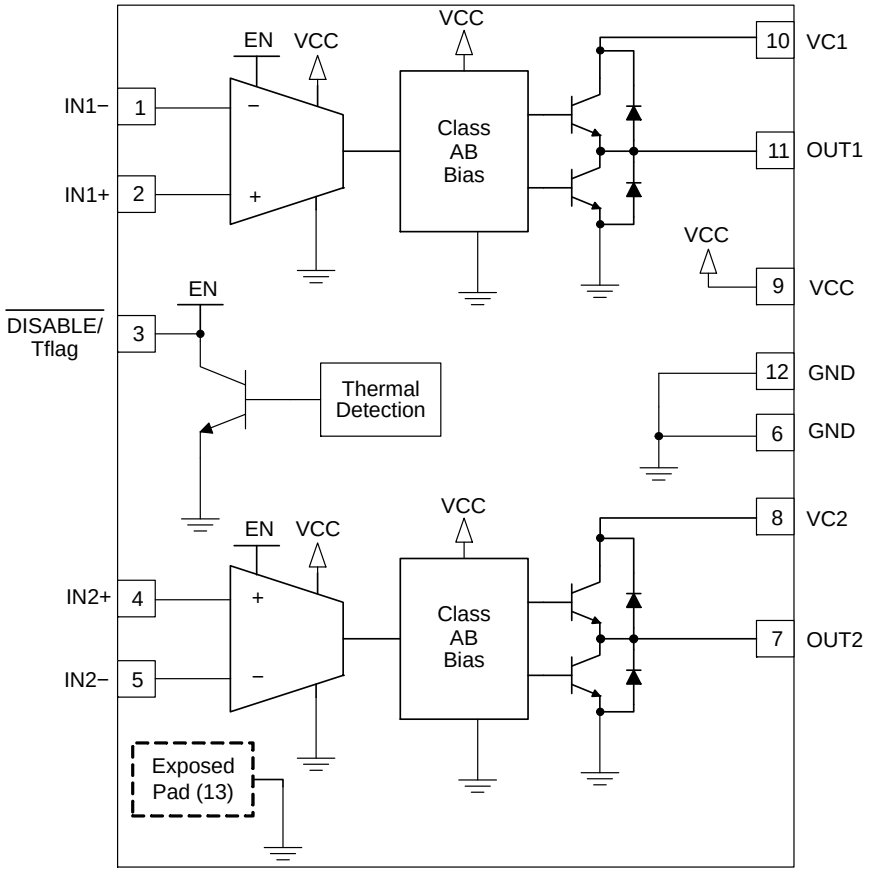



**Figure 1. Block Diagram**

**Table 1. PIN DESCRIPTION**

| Pin | Name | Type | Description |
|---|---|---|---|
| 1 | IN1− | Input | Negative input of amplifier 1. |
| 2 | IN1+ | Input | Positive input of amplifier 1. |
| 3 | $\overline{\text{DISABLE}}$/Tflag | Input/Output | Dual use pin −Thermal flag− an open collector output requiring an external pull−up resistor. The output is pulled low when the thermal limit is reached. It is high−impedance in normal operation.<br>Disable − Must use an open collector/drain for input with pull−up resistor to Vcc. Pulling pin low disables the amplifiers. If pin is not used, a pull−up resistor to Vcc is still required (10 KΩ recommended) |
| 4 | IN2+ | Input | Positive input of amplifier 2. |
| 5 | IN2− | Input | Negative input of amplifier 2. |
| 6 | GND | Power | Power ground. |
| 7 | OUT2 | Output | Output of amplifier 2. |
| 8 | VC2 | Power | Positive supply of output stage 2. |
| 9 | VCC | Power | Positive supply of core circuitry. |
| 10 | VC1 | Power | Positive supply of output stage 1. |
| 11 | OUT1 | Output | Output of amplifier 1. |
| 12 | GND | Power | Power ground. |
| 13 | EXPOSED PAD | Power | The Exposed Pad must be attached to a heat−sinking conduit and **connected to GND**. |

**Table 2. ABSOLUTE MAXIMUM RATINGS** Over operating free−air temperature, unless otherwise stated

| Parameter | Symbol | Limit | Unit |
|---|---|---|---|
| Supply Voltage ($V_{CC}$ − GND) | $V_{CC}$ | 16 | V |
| Output Supply Voltage | VC1, VC2 | 16 | V |
| **INPUT AND OUTPUT PINS** | | | |
| Differential Input Voltage | $V_{id}$ | $\pm V_{CC}$ | V |
| Input Common Mode Voltage Range | $V_{ICR}$ | −0.3 to $V_{CC}$ +0.3 | V |
| Output Current (Note 1) | $I_{OUT}$ | ±1000 | mA |
| DISABLE/Tflag Pin Voltage (Note 2) | $V_{DISABLE/Tflag}$ | 7 | V |
| **TEMPERATURE** | | | |
| Storage Temperature | $T_{STG}$ | −65 to 165 | °C |
| Junction Temperature | $T_{J(MAX)}$ | 150 | °C |
| **ESD RATINGS (Note 3)** | | | |
| Human Body Model | HBM | ±1500 (IN−, Tflag pins).<br>±2000 (All other pins) | V |
| Machine Model | MM | ±150( IN−, Tflag pins).<br>±200 (All other pins) | V |
| Charge Device Model | CDM | ±2500 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Continuous short−to−ground or source; power dissipation must be taken into consideration.
2. Connected to voltage source via a pull−up resistor.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JEDEC standard: JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (JEDEC standard: JESD22−A115)
   ESD Charged Device Model tested per ANSI/ESD S5.3.1−2009 (AEC−Q100−011)

**Table 3. THERMAL INFORMATION** (Note 4)

| Thermal Metric | Symbol | Limit | Unit |
|---|---|---|---|
| Junction to Ambient – UDFN12<br>(Exposed pad connected to 50 $mm^2$ one ounce copper.) | $\theta_{JA}$ | 147 | °C/W |
| Junction to Ambient – UDFN12<br>(Exposed pad connected to 1200 $mm^2$ one ounce copper.) | $\theta_{JA}$ | 52 | °C/W |

4. Based on JEDEC.

**Table 4. RECOMMENDED OPERATING CONDITIONS**

| Parameter | Symbol | Limit | Unit |
|---|---|---|---|
| Operating Supply Voltage | $V_{CC}$ | 3.3 to 13.2 | V |
| Output Supply Voltage | VC1, VC2 | 3.3 to 13.2 | V |
| Output Current (Note 5) | IC1, IC2 | ±500 | mA |
| Operating Temperature Range | $T_A$ | −40 to +125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Power dissipation must be taken into consideration to avoid thermal shutdown.

**Table 5. ELECTRICAL CHARACTERISTICS: $V_{CC}$ = VC1 = VC2 = 5 V**
**Boldface** limits apply over the specified temperature range, $T_A$ = –40°C to +125°C.
At $T_A$ = +25°C, $R_L$ = 1 kΩ connected to midsupply, $V_{OUT}$ = midsupply, unless otherwise noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | |
| Offset Voltage | $V_{OS}$ | | | 1 | 15 | mV |
| Offset Voltage Drift | δV/δT | | | 2 | | μV/°C |
| Input Bias Current | $I_{IB}$ | | | 550 | 1000 | nA |
| Input Offset Current | $I_{OS}$ | | | 10 | 100 | nA |
| Input Common Mode Range (Note 6) | $V_{CM}$ | | 0 | | **3.8** | V |
| Common Mode Rejection Ratio | CMRR | | 90 | 100 | | dB |
| **OUTPUT CHARACTERISTICS (OUT1, OUT2)** | | | | | | |
| Output Voltage High (Note 7) | $V_{OH}$ | $V_{id}$ = 1 V, $I_O$ = +250 mA | 4.0 | 4.15 | | V |
| Output Voltage Low | $V_{OL}$ | $V_{id}$ = −1 V, $I_O$ = −250 mA | | 200 | 350 | mV |
| **DYNAMIC PERFORMANCE** | | | | | | |
| Open Loop Voltage Gain | $A_{VOL}$ | | 90 | 105 | | dB |
| Gain Bandwidth Product | GBWP | $R_L$ = 47 Ω, $C_L$ = 100 nF | | 350 | | kHz |
| Gain Margin | $A_M$ | $R_L$ = 47 Ω, $C_L$ = 100 nF | | 6 | | dB |
| Phase Margin | ψM | $R_L$ = 47 Ω, $C_L$ = 100 nF | | 45 | | ° |
| Slew Rate | SR | | | 1.5 | | V/μs |
| **POWER SUPPLY** | | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_{CC}$ = VC1 = VC2 = 3.3 V to 13.2 V | 65 | 75 | | dB |
| Quiescent Current (Operating) | $I_{CC}$ | No $R_L$, $C_L$ = 100 nF | | 3 | 4 | mA |
| Quiescent Current (Output) | $I_{C1}$, $I_{C2}$ | (Per op amp) No $R_L$, $C_L$ = 100 nF | | 4 | 6 | mA |
| **THERMAL CHARACTERISTICS** | | | | | | |
| Thermal Shutdown (Note 8) | $T_{SHUTDOWN}$ | | | 160 | | °C |
| **LOGIC CHARACTERISTICS ($\overline{\text{DISABLE}}$/Tflag)** | | | | | | |
| Output Voltage Low (Note 6) | $V_{OL}$ | $I_{OL}$ = 1 mA | | | 0.7 | V |
| Input Voltage High (Note 9) | $V_{IH}$ | | 1.5 | | | V |
| Input Voltage Low (Note 10) | $V_{IL}$ | | | | 1.1 | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
6. $V_{CM}$ is a function of $V_{CC}$ ($V_{CC}$ – 1.2 V).
7. $V_{OH}$ is a function of $V_{CC}$ ($V_{CC}$ − 0.8 V).
8. Guaranteed by design/characterization.
9. $\overline{\text{DISABLE}}$/Tflag pin with a pull−up resistor for sourcing.
10. $\overline{\text{DISABLE}}$/Tflag pin with an open collector/drain for sinking.

## TYPICAL CHARACTERISTICS

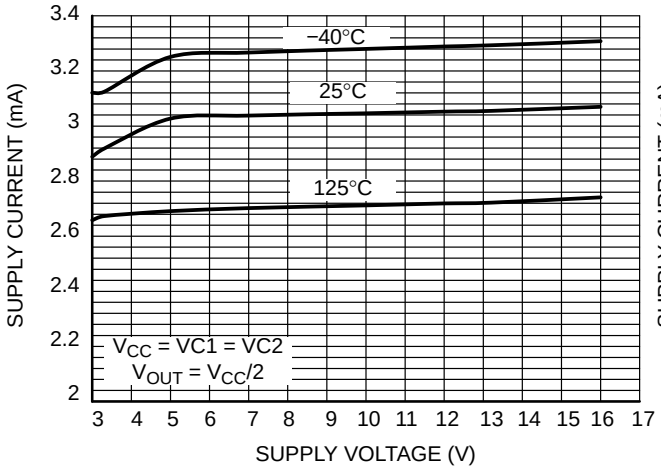



**Figure 2. $I_{CC}$ Quiescent Current vs. Supply Voltage over Temperature**

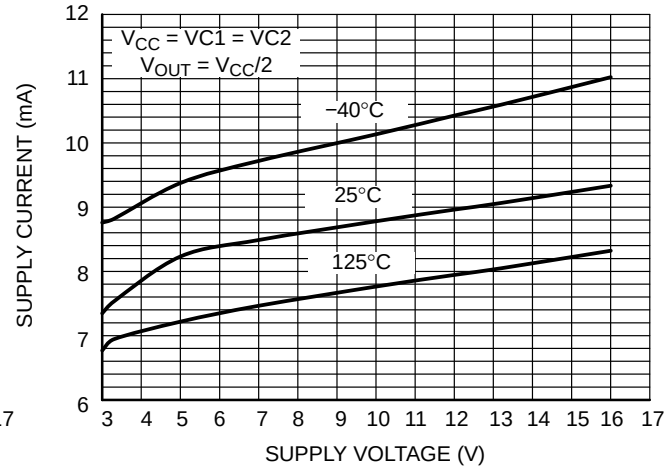



**Figure 3. Ic Quiescent Current vs. Supply Voltage over Temperature (Ic1, Ic2 combined)**

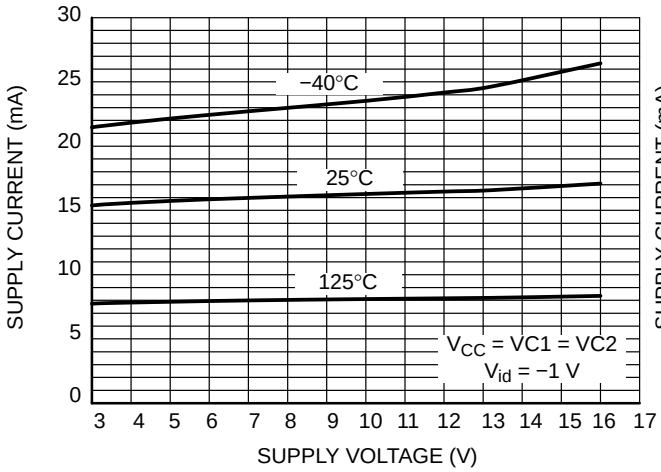



**Figure 4. Comparator Mode (Negative), $I_{CC}$ Quiescent Current vs Supply Voltage**

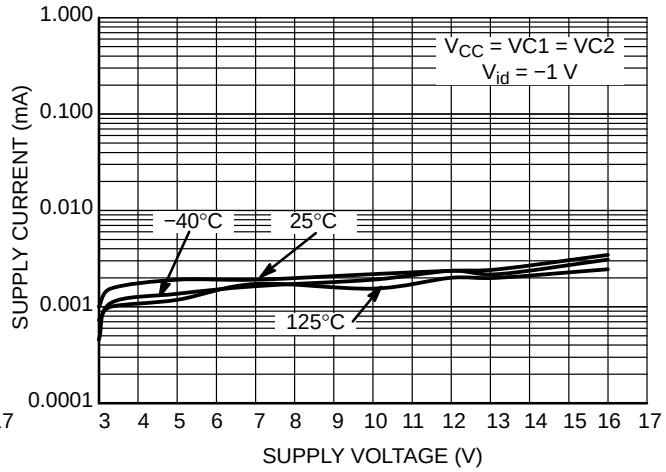



**Figure 5. Comparator Mode (Negative), Ic Quiescent Current vs Supply Voltage (Ic1,Ic2 Combined)**

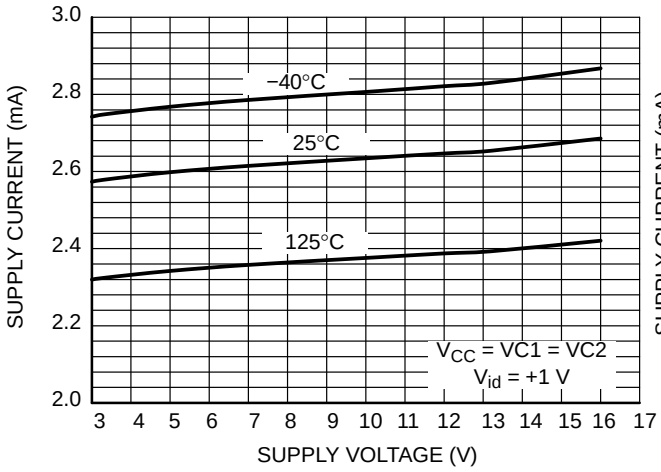



**Figure 6. Comparator Mode (Positive), $I_{CC}$ Quiescent Current vs Supply Voltage**

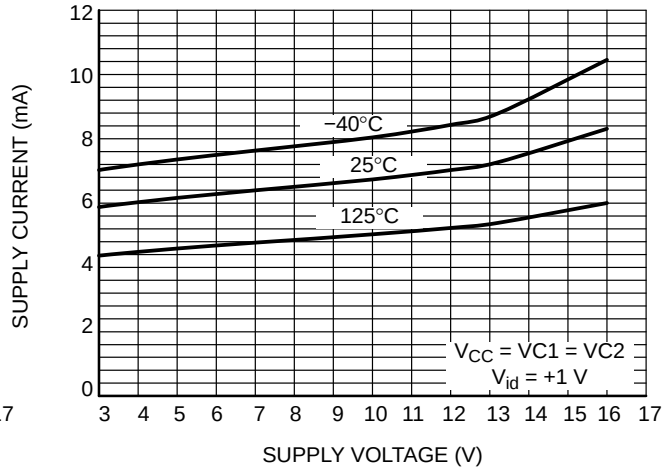



**Figure 7. Comparator Mode (Positive), Ic Quiescent Current vs Supply Voltage (Ic1,Ic2 Combined)**

## TYPICAL CHARACTERISTICS

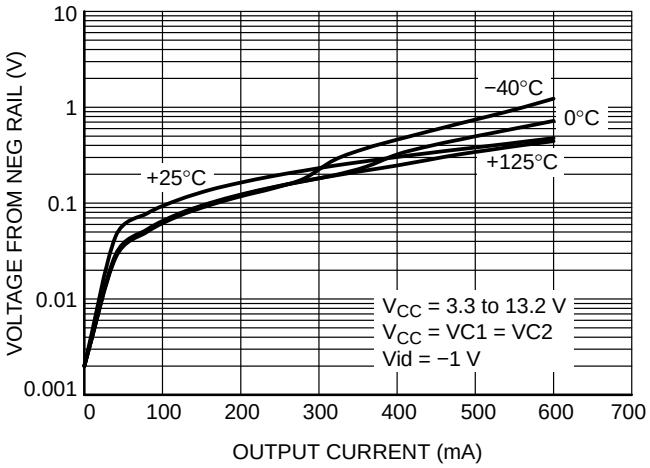



**Figure 8. Low Level Output Voltage vs. Output Current Over Temperature**

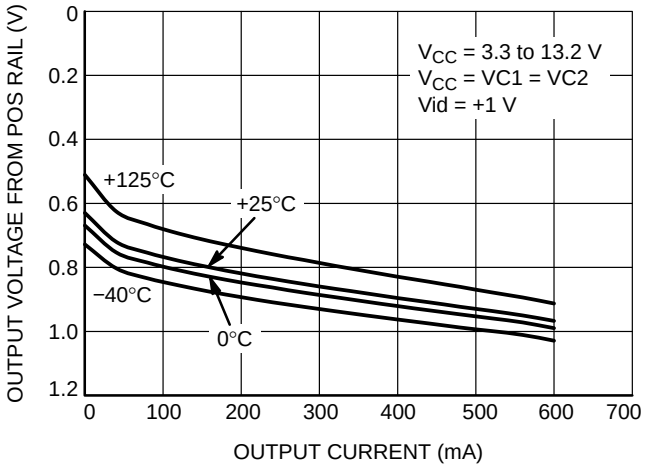



**Figure 9. High Level Output Voltage vs. Output Current Over Temperature**

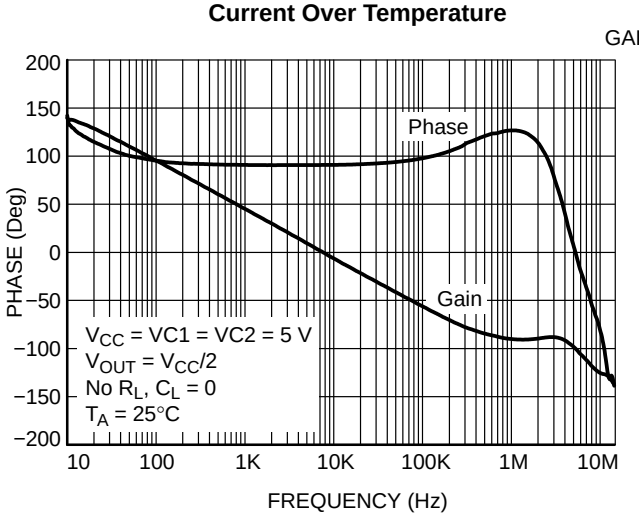



**Figure 10. Open Loop Gain/Phase (No $R_L$, $C_L$ = 0)**

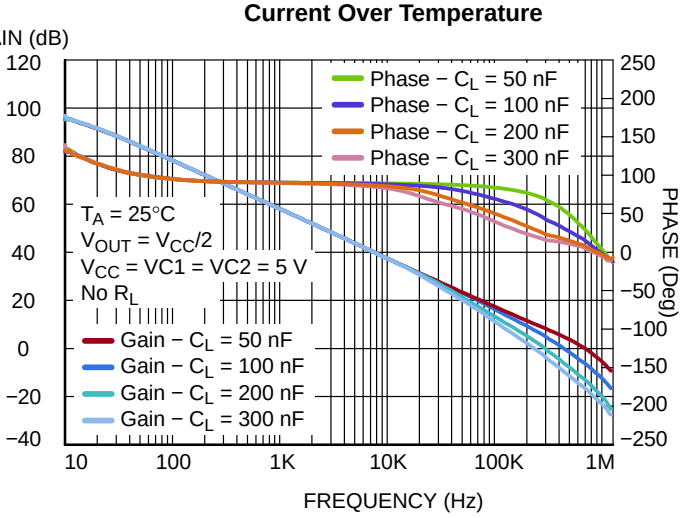



**Figure 11. Open Loop Gain/Phase (No $R_L$, $C_L$ = Varied)**

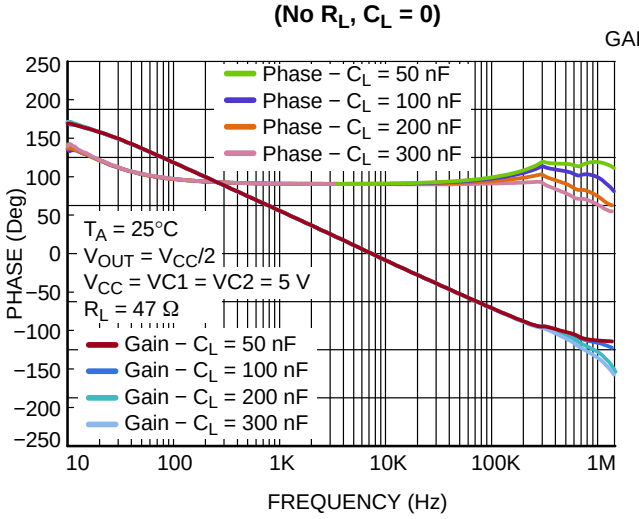



**Figure 12. Open Loop Gain/Phase ($R_L$ = 47 Ω, $C_L$ = Varied)**

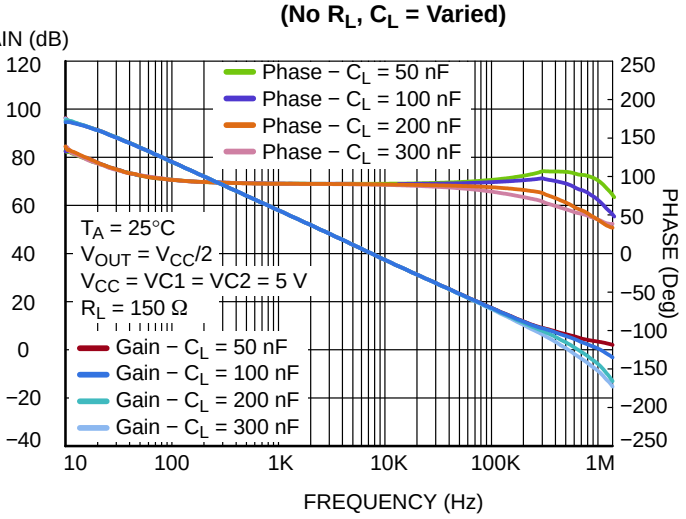



**Figure 13. Open Loop Gain/Phase ($R_L$ = 150 Ω, $C_L$ = Varied)**

## TYPICAL CHARACTERISTICS

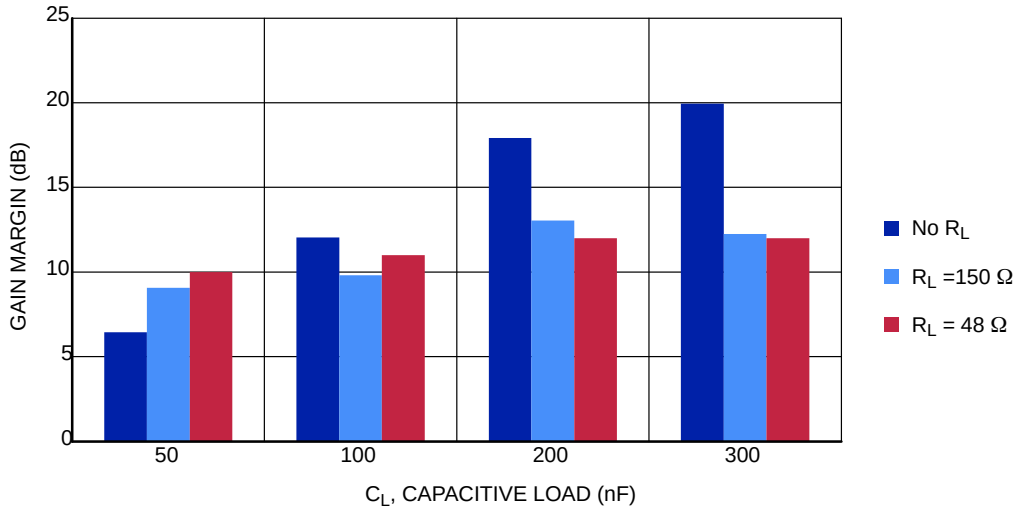



**Figure 14. Gain Margin vs. Load**

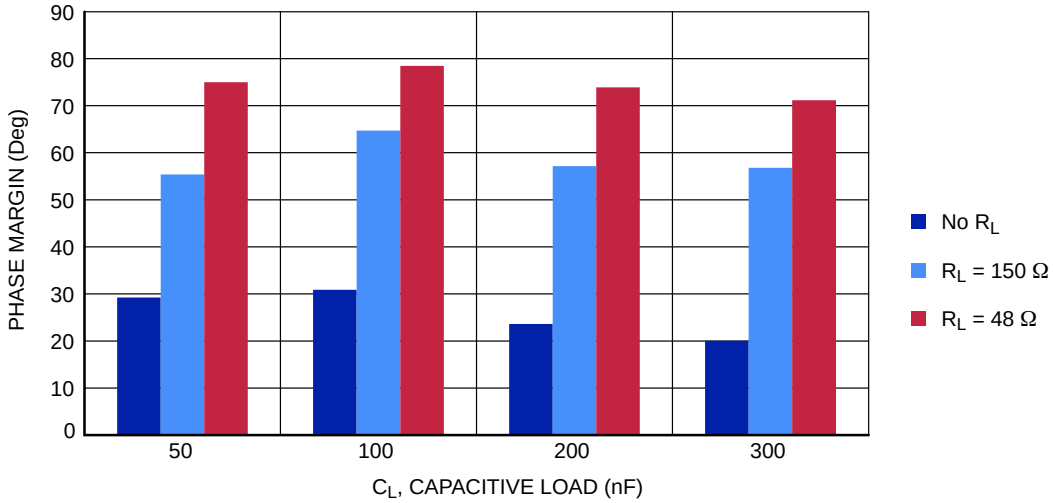



**Figure 15. Phase Margin vs. Load**

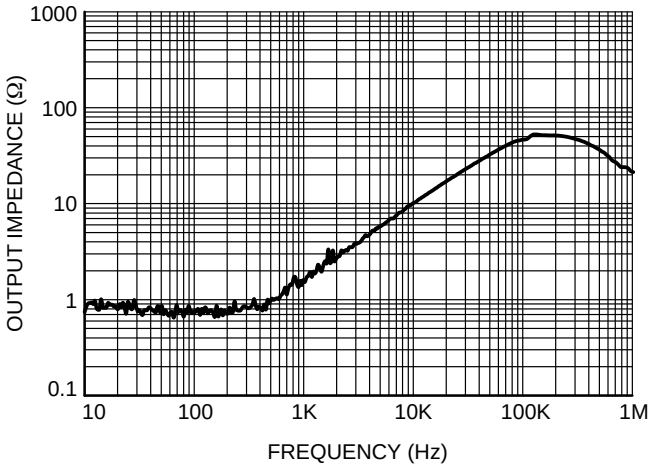



**Figure 16. Open Loop Output Impedance vs. Frequency**

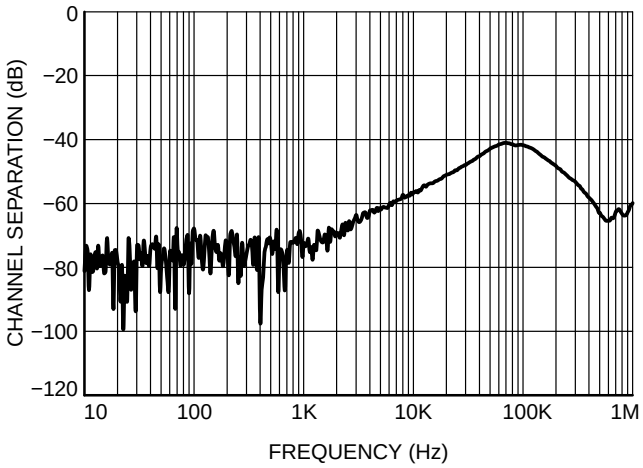



**Figure 17. Channel Separation vs. Frequency**

## TYPICAL CHARACTERISTICS

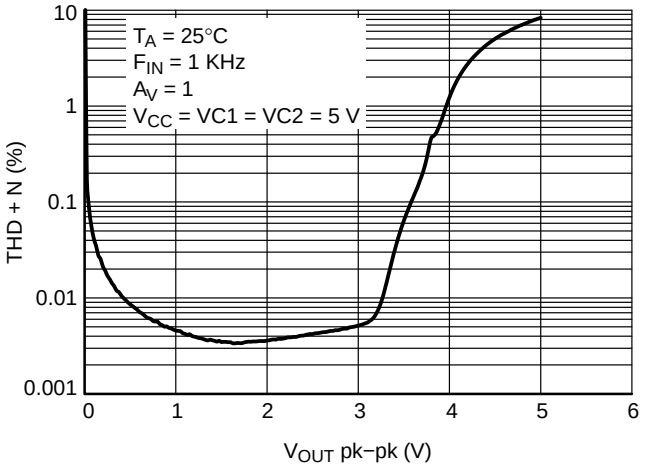



**Figure 18. Total Harmonic Distortion + Noise vs. Vout**

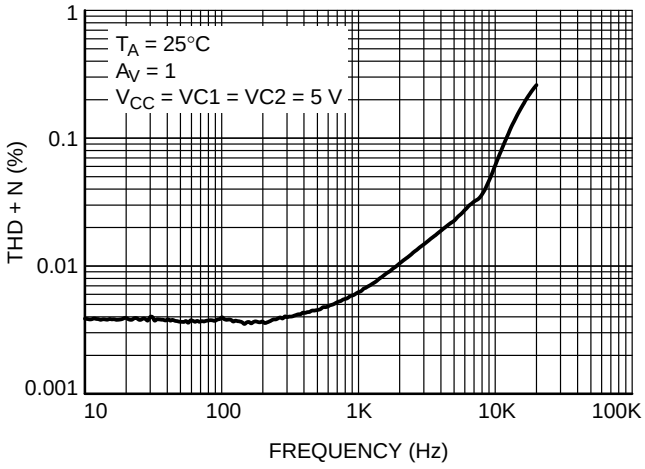



**Figure 19. Total Harmonic Distortion + Noise vs. Frequency**

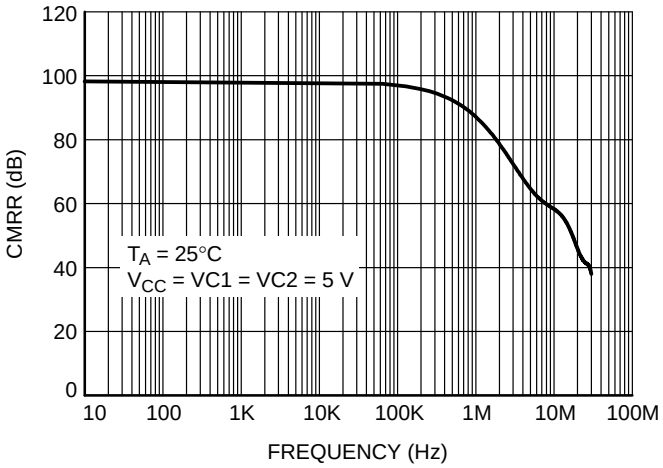



**Figure 20. CMRR vs. Frequency**

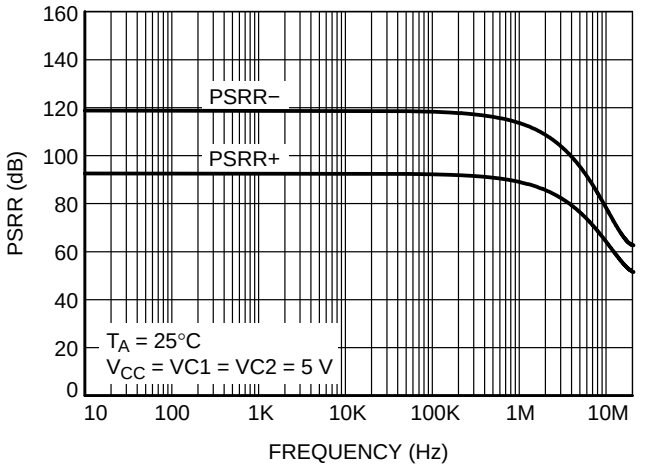



**Figure 21. PSRR vs. Frequency**

## APPLICATIONS INFORMATION

Figure 22 shows a typical application on how to connect the NCx5652 pins where the $V_{CC}$ is supplied by 5 V and the output stages are supplied with 12 V. In this configuration the inputs can be driven up to 3.8 V. The outputs can be as high as 4 V and able to go near ground due to the excellent $V_{OL}$ parameters. The loads can be up to 500 mA continuous.

### Power Supply

The supply pins should be properly bypassed with ceramic 0.1 μF to 1 μF capacitors. The different supply pins for the input stage ($V_{CC}$) and the output stage (VC1,VC2) provide a flexible power option. In many applications there is often a digital supply and different supply for driving motors or elements. The output stage can be optimized for the voltage requirements of the load. There are no requirements on the voltage levels (as long as they are within specification) and sequencing of the $V_{CC}$, VC1, and VC2 pins. It should be noted that the input and output swings are a function of $V_{CC}$. The common mode voltage range and output swings are specified in the electrical section according to the $V_{CC}$ voltage.

### Shutdown Feature

The NCx5652 provides a thermal shutdown feature to protect the device during fault conditions. Pin 3 is an open collector output that can be connected to a microcontroller to alert the system that a thermal shutdown has occurred. When the device is in a thermal shutdown condition, the outputs are tri−stated. The same pin can be used for an input as well. It can be open collector OR'd so that the microcontroller can disable the device by driving this pin low. This pin must always be pulled high via a 10 kΩ resistor (recommended value). It should always be driven with an open collector/drain device. Some microcontrollers have open drain configurable outputs.

### Stability

The NCx5652 is designed to drive large capacitive loads and not oscillate even at unity gain. It is recommended that a minimum of 0.1 μF capacitor be placed on the outputs to ensure stability. This is mainly required for no load or light load conditions. If configuring the device as an emitter follower, it is also recommended to use a 10 kΩ feedback resistor as shown in **Figure 22**.

### Thermal Considerations

As power in the NCx5652 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCS5652 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCx5652 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \qquad \text{(eq. 1)}$$

Since $T_J$ is not recommended to exceed 150°C, then the NCx5652 soldered on 1200 $mm^2$, 1 oz copper area, FR4 can dissipate up to 2.5 W when the ambient temperature ($T_A$) is 25°C.

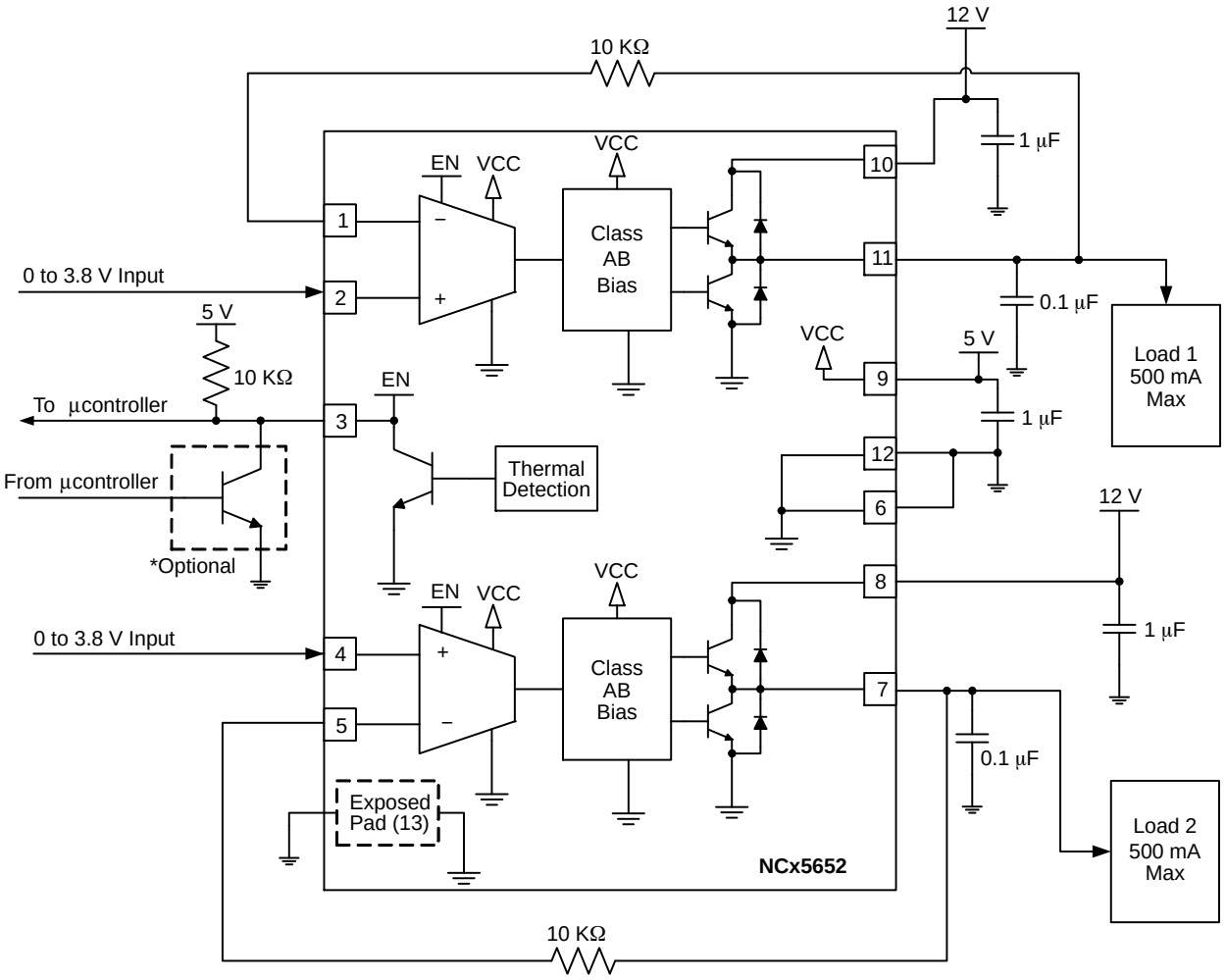



**Figure 22. NCx5652 Application Diagram**

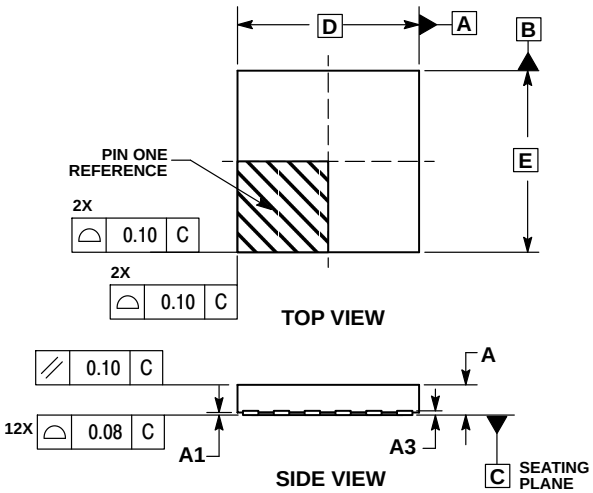
## ORDERING INFORMATION

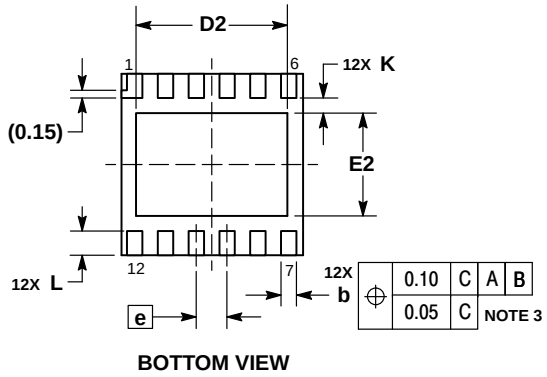
| Device | Automotive | Marking | Package | Shipping † |
|---|---|---|---|---|
| NCS5652MUTWG | No | N5652 | UDFN12, 3x3 mm<br>Pb−Free | 3000 / Tape & Reel |
| NCV5652MUTWG | Yes | N5652 | UDFN12, 3x3 mm<br>Pb−Free | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

**UDFN12 3x3, 0.5P**
CASE 517AM−01
ISSUE O

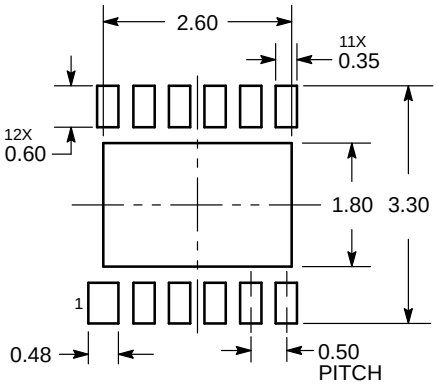



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.45 | 0.55 |
| A1 | 0.00 | 0.05 |
| A3 | 0.07 REF | |
| b | 0.20 | 0.30 |
| D | 3.00 BSC | |
| D2 | 2.40 | 2.60 |
| E | 3.00 BSC | |
| E2 | 1.60 | 1.80 |
| e | 0.50 BSC | |
| K | 0.20 | −−− |
| L | 0.30 | 0.50 |

**SOLDERING FOOTPRINT***




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



**PUBLICATION ORDERING INFORMATION**

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